transistors for activating respective ones of said access transistors [upon receipt of] in response to a selection signal for selecting one of said memory cells[,]; and

a differential sense amplifier for reading from and writing to said memory cells, said sense amplifier having a first input connected to said bit line, and a second input connected to receive a reference signal, said sense amplifier having a data [input/output] input terminal and a data output terminal, said sense amplifier for differentially [driving] comparing signals on said first and second input lines for reading a data state from a selected one of said memory cells, [connected thereto] and for applying [the] a data state [thus] read from said selected memory cell to said [input/output] data output terminal, and said sense amplifier for driving said bit [lines] line connected to said selected memory cell to one of a set of predetermined voltage states corresponding to a data state received at said [input/output] data input terminal for writing said received data state into the selected one of said memory cells.

63. (Amended) A non-volatile memory circuit as recited in claim 61 including a respective complementary memory cell [for] associated with each memory cell of said plurality of memory cells, wherein [the] an output of the corresponding complementary memory cell is transmitted [through] by a bit line to provide said reference signal to said sense amplifier.

66. (Amended) A non-volatile memory cell as recited in claim 61 including a dummy ferroelectric capacitor memory cell [for] associated with said plurality of memory cells, and a bit line connected to provide [the] an output of the dummy memory cell as the reference signal to said sense amplifier.

67. (Amended) A non-volatile memory circuit, comprising:

a plurality of memory cells each [comprising] including a ferroelectric capacitor connected in series with an access transistor, said plurality of memory cells being connected between a plurality of respective bit lines and a common drive line,

a word line connected to control terminals of said access transistors for activating said transistors [upon receipt of] in response to a selection signal for selecting one of said memory cells, and

a plurality of differential sense amplifiers corresponding respectively to said bit lines for reading from and writing to [said] memory cells associated with the bit lines, each sense amplifiers having a first input connected to the corresponding bit line and a second input connected to receive a reference signal, each said sense amplifier having a data input/output terminal, said sense amplifiers for differentially [driving] comparing signals on said first and second inputs thereof for reading a data state from the one of said memory cells connected thereto, and for applying [the] a data state [then] read from said selected memory cell to said [input/output] output terminal, and said sense amplifiers for driving the corresponding bit lines connected to said memory cells to predetermined voltage states corresponding to a data state received at said [input/output] input terminal for writing said received data state into the corresponding one of said memory cells.